



SPEAR: Scalable Panels for Efficient, Affordable Radar

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Outline

- 👉 Low Power Density Radar System Considerations
- ◆ The SPEAR Program
- ◆ Low Cost Panel Technologies
- ◆ Summary

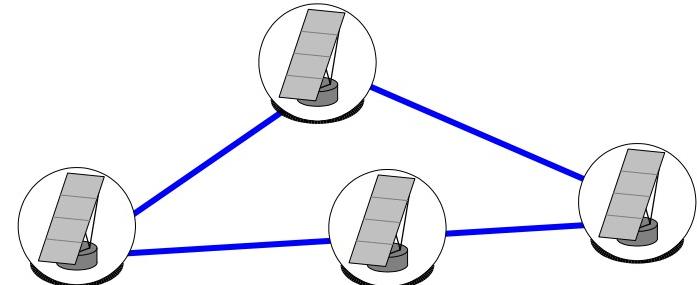
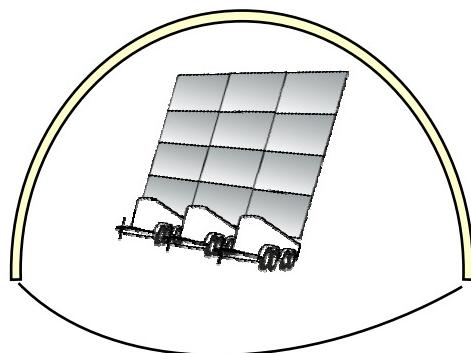
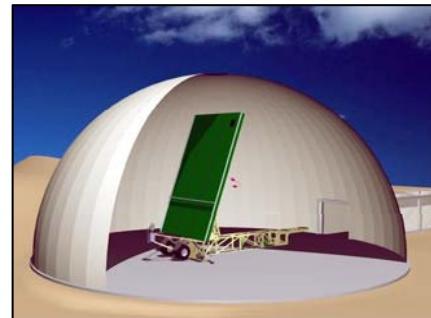
SPEAR is a prime example of an application of low-cost manufacturing technologies in a next-generation military system

Next Generation Radar for BMDS

2000



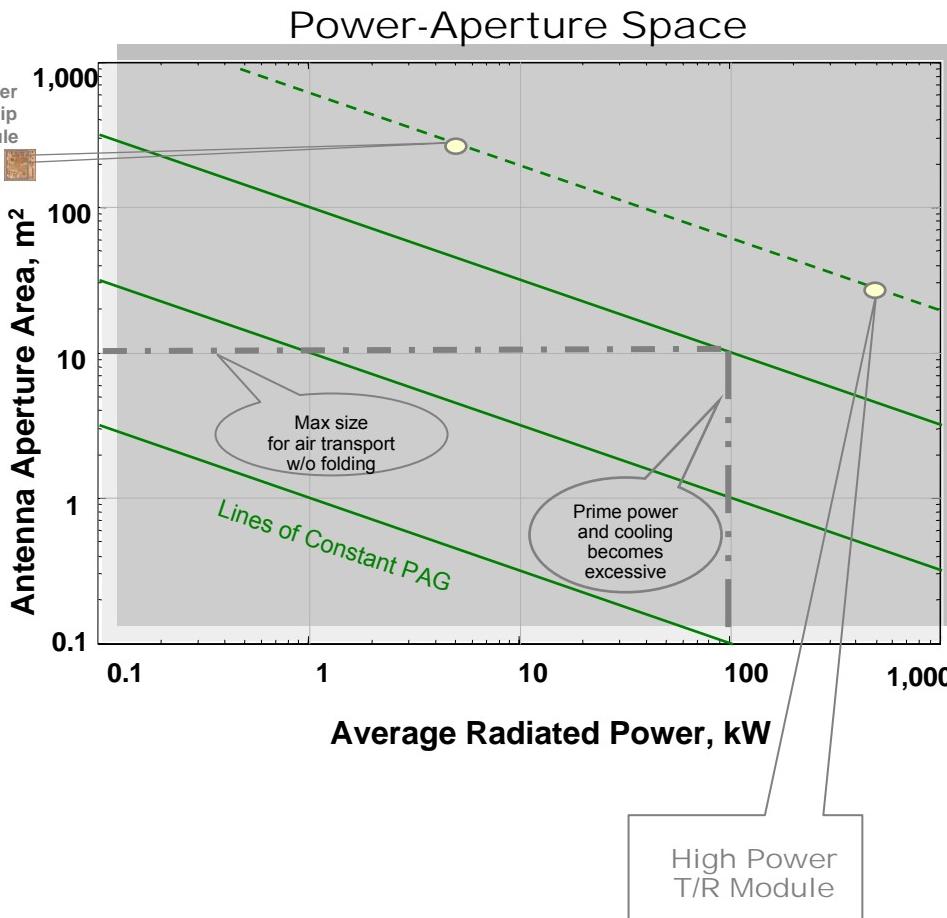
2010



Next Generation Radar (NGR) to provide objective BMDS capabilities

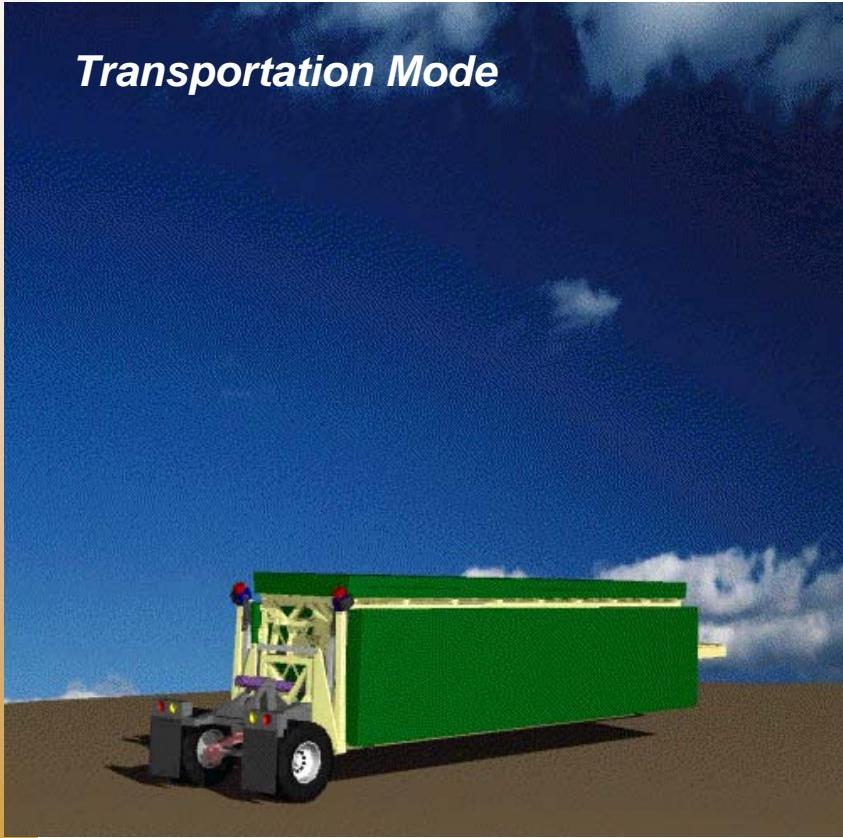
How can we achieve future needs for affordable, transportable radars?

- ◆ Driving performance is tracking/discrimination sensitivity
- ◆ Radar figure of merit is PAG (power · aperture · gain)
- ◆ For solid state (active) arrays:
 - $P = \text{Power per element } (P_e) \times \text{number of elements } (N)$
 - $A = \text{Area per element } (A_e) \times \text{number of elements } (N)$
 - $G = 4\pi A_e N / \lambda^2$
- ◆ So $\text{PAG} = 4\pi (A_e)^2 N^3 P_e / \lambda^2$
- ◆ To improve performance, grow one of these:
 - A_e = area of one element (GBR-P)
 - ❖ LFOV
 - ❖ Too large to transport
 - P_e = power per element (GaN, SiC approach)
 - ❖ Cooling becomes serious problem for transportability
 - ❖ Prime power becomes excessive for transportability
 - ❖ T/R module cost is excessive
- ◆ Or, LPD Approach → Break out of the box by:
 - Grow A by increasing N (third power payoff)
 - ❖ FFOV
 - Reduce P_e (**P_e goes as $1/N^3$**)
 - ❖ Reduced cost per element ($<\$10$)
 - ❖ Cooling and prime power requirement decrease significantly
 - ❖ Aperture will not be as mechanically rigid
 - ❖ But, large aperture can be folded for stowage

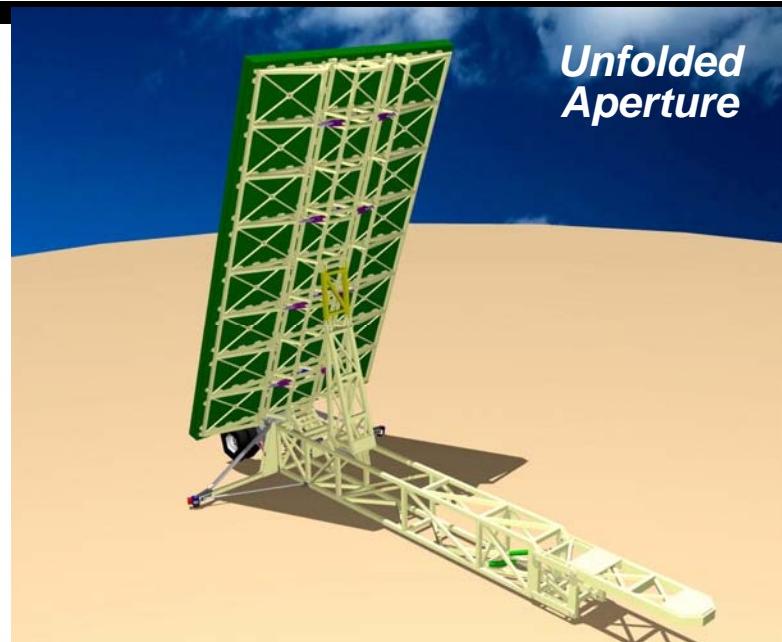


Example of Deployable Structure

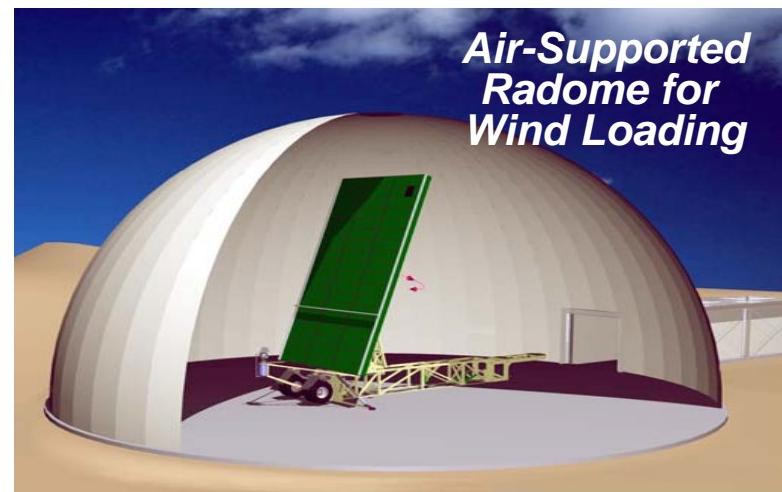
Transportation Mode



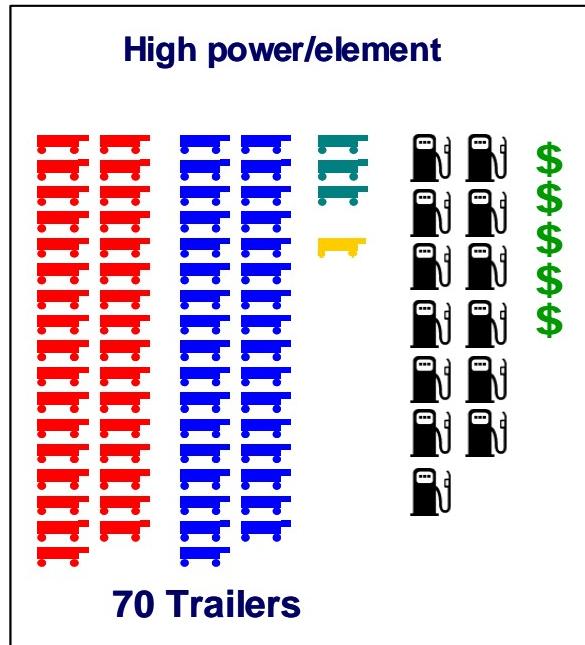
Unfolded Aperture



Air-Supported Radome for Wind Loading



Benefits of LPD Antenna Technology



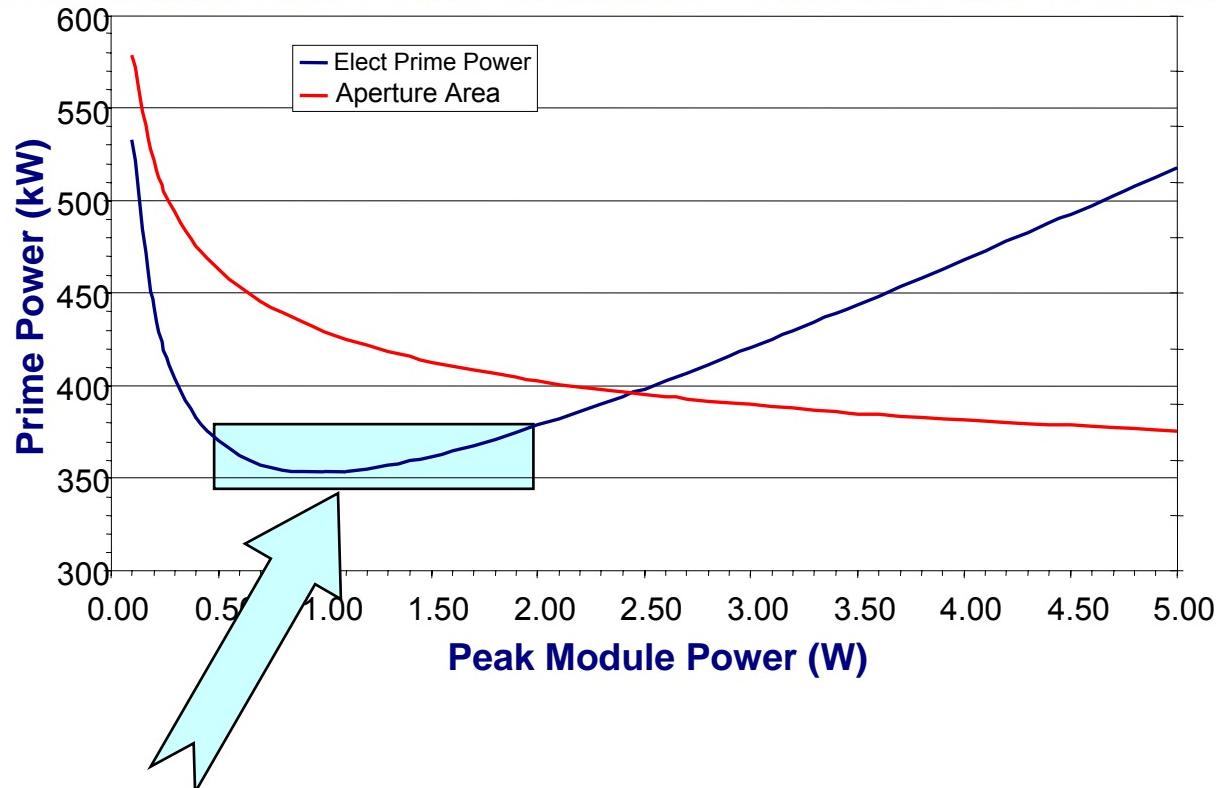
Key:

- Heat Exchanger
- Power Generator
- Antenna & Electronics
- Control/Processing
- Fuel Rate
- Cost

Large LPD antennas reduce cost and system footprint

What is the optimum power density?

Electronics Prime Power vs Module Power for Base Unit Fixed PAG



Region of interest for SPEAR IPT

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SPEAR Vision

Scalable Panels for Efficient, Affordable Radars for BMDS



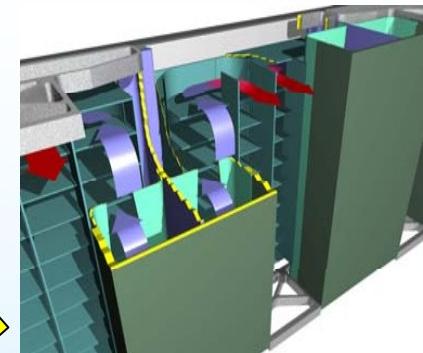
Alignment and Calibration

Single Chip
T/R



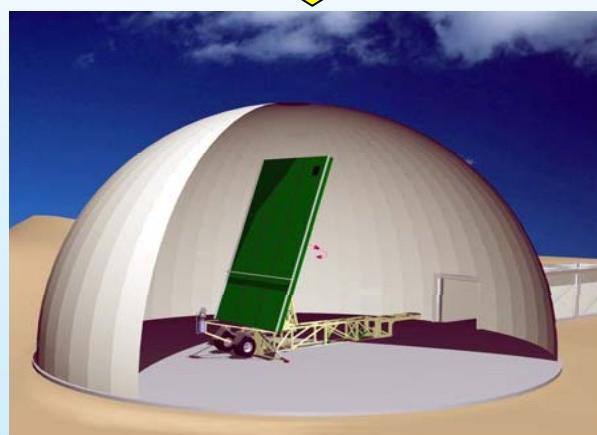
AFRL Scalable Panel

Efficient Cooling



Risks

- Transportable, Lightweight, Deployable Structure
- Alignment and Calibration of Deployed Structure
- Wind Loading of Large Aperture
- Cost of Low Power Panels
- Efficient, Reliable Cooling

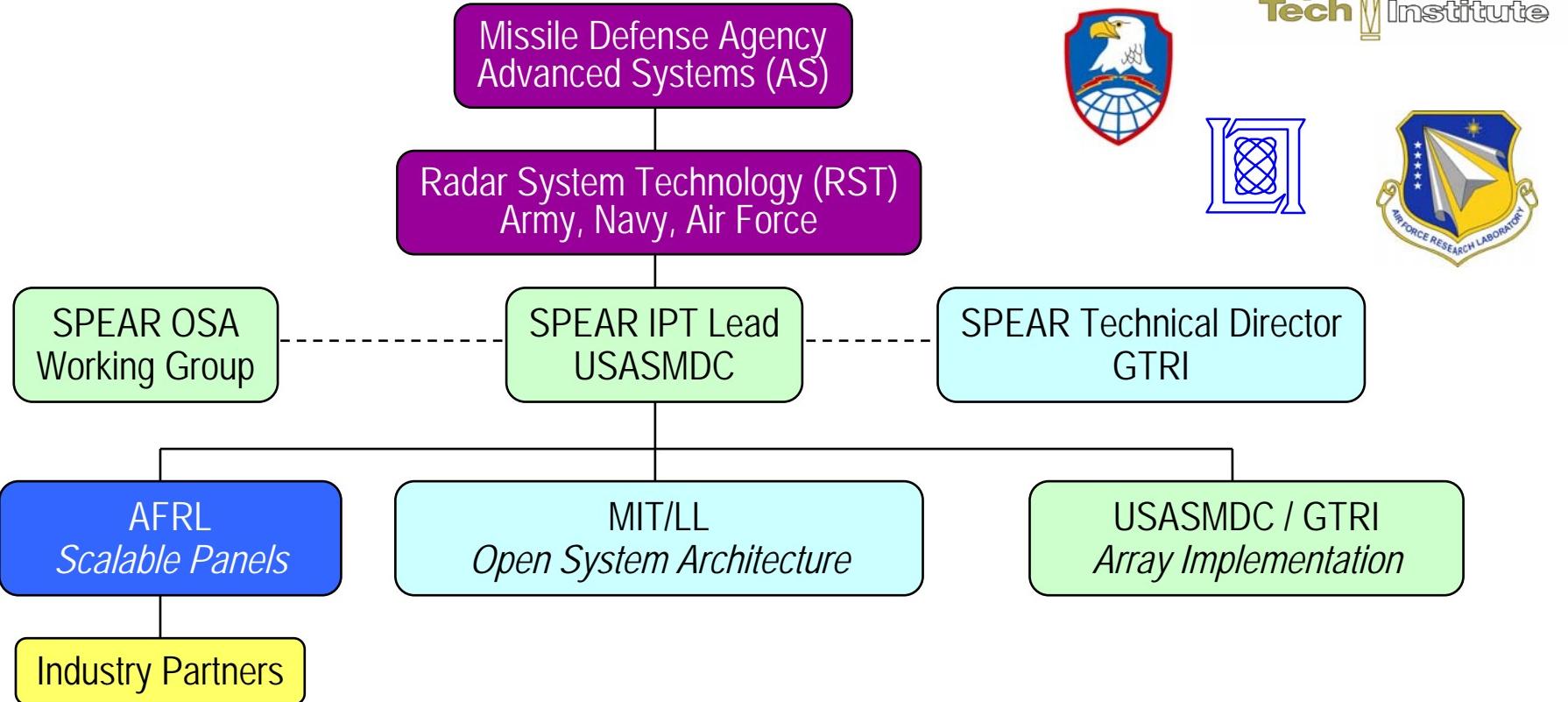


Transportable, Deployable Structure

Benefits

- Full Field-of-View
- Affordable
- 30-day Relocation
- Low Power Density
- Efficient
- Enhanced Bandwidth

SPEAR IPT



MDA/AS RST tri-service panel established IPT to leverage space, airborne (AFRL) and ground based radar (USASMDC/GTRI) expertise to develop affordable scalable panels with a government owned interface standard (MIT/LL OSA)

SPEAR Spiral Development

2002 2003 2004 2005 2006 2007 2008 2009 2010

Scalable Array

Scalable Radar

Gov't & Industry IPT

- Leads Development
- System Engineering
- Open Standards

Tech Dev For Spiral 1

- Distributed Processing
- Alignment/Calibration
- Coherency
- Affordability
- Thermal
- Sub-array Fab.

Tech Dev For Spiral 2

- Distributed Array Techniques
- WB Rx/Tx on a chip
- WB DBF Panel (AF \$ support)

Specification Development

Solicitation
4Q FY04

Contracts
Jan 2005

Tech Development

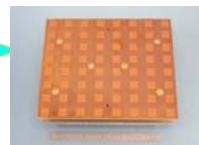
Analog Testbed

- Testbed
- OSA
 - Panel Spec
 - Approach Selection

Spiral 1 FY05/06

Spiral 1 Testbed

- Antenna
- Analog panels
 - Digital receivers

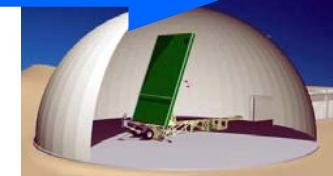


Antenna
Sub-Arrays

Spiral 2 FY 07

Spiral 2 Demonstrator

- Radar
- Digital panels
 - Distributed



Radar
Demonstrator



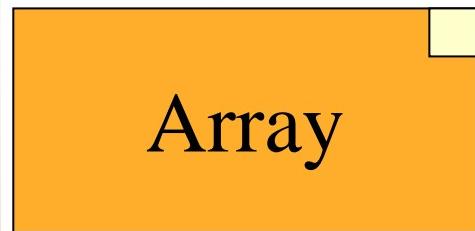
Antenna
Testbed

Outline

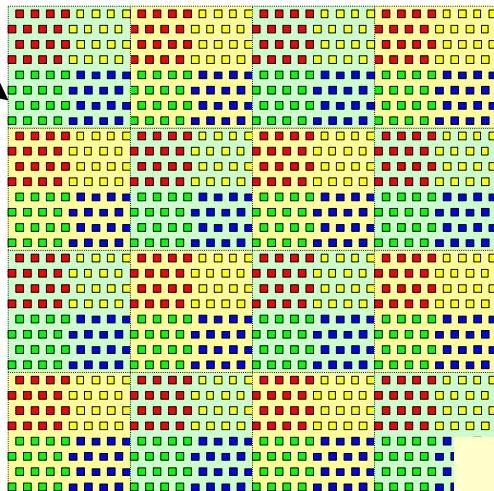
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NGR/SPEAR Study Results: Base Unit Antenna Notional Designs

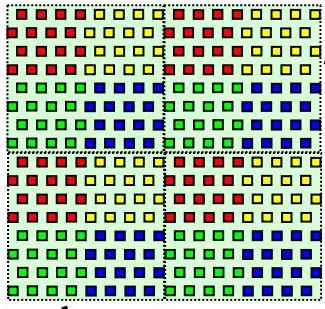
Approach



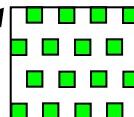
Autonomous Panel
2x2 Digital Sub-Arrays
0.5m x 0.5m



Digital Sub-Array (DSA)
4x4 analog sub-arrays
0.25m x 0.25 m

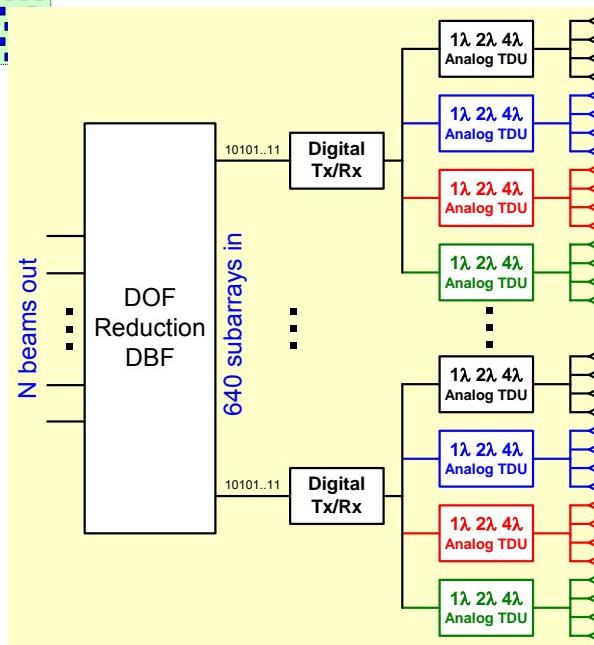


Analog Sub-Array (ASA)
4x4 Elements



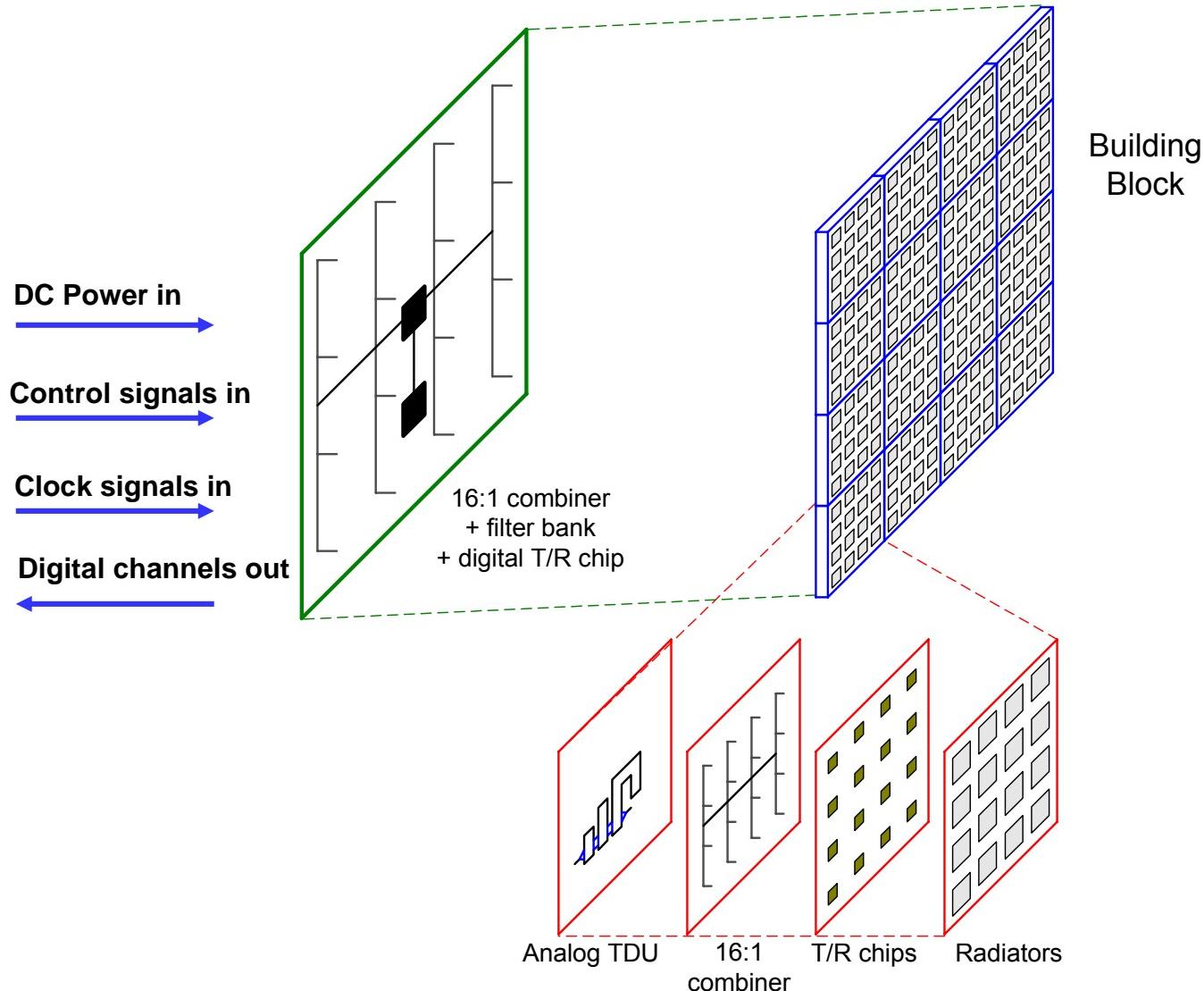
Baseline Design

- 4 x 4 element Analog Subarray (ASA)
- 16 x 16 element Digital Subarray (DSA)
- 1024 elements per panel (4 DSAs)
- Wide Operating Bandwidth
 - ◆ Analog time delay for short bits (1λ , 2λ , 4λ)
 - ◆ Digital time delay for longer bits
- Full Field-of-View
- DOF Reduction beamformer from 100's of DSAs to 10's of beams



Building Block

(= 1 Digital Subarray - 16X16 Elements)



Low Cost Panel Technologies

- ◆ Emphasis on using established industry processes
 - Circuit board based signal and power distribution
 - Use of flex materials and HDI for higher density and lower mass
 - Maximizing automation over hand assembly
 - Possible use of plastic or non-hermetic packaging approaches
- ◆ Better understanding of packaging tradeoffs and how they affect cost
 - Greater single chip integration vs multiple chips
 - Single chip vs multichip modules
 - Including more routing on modules vs on the circuit board

Ceramic Package Option

Panel Cross Section with Ceramic Packaged MMICs



- ◆ Printed Circuit Board (PCB) Technology for RF Distribution and DC Bias Networks
- ◆ Hermetic Cavity Package for MMICs (Mature Technology)
- ◆ Single or Multichip modules
- ◆ Most Routing in PCB Reduces Number of Layers in Ceramic (Lower Cost)
- ◆ Multiple Ceramic Module Attach Approaches (pins, fuzz button, BGA)
 - Can be Automated
 - Lower Cost

Plastic Package Approach

Panel Cross Section with Plastic Packaged MMICs



- ◆ Plastic Molded Packages Offer a Very Low Cost Option for Some Applications
- ◆ Some Materials Compatible with X-Band Frequency Range
- ◆ Non-Hermetic
- ◆ Coatings Such as BCB or Parylene Provide Chip Protection
- ◆ Direct or BGA Attach
- ◆ Additional PCB Layers Required for Signal Routing
- ◆ Liquid Crystal Polymers (LCP) Can Provide Hermeticity but are Less Mature

Packageless Approach

Panel Cross Section with MMICs Mounted to PCB in a Packageless Approach



- ◆ MMICs Mounted Directly to the PCB Surface
 - Flip Chip Mount (requires underfill)
 - Adhesive Mount w/ Wire Bonding (chip face up)
 - Both Approaches Require Chip Protection Method (to be developed)
- ◆ All RF and DC Routing are in the PCB
- ◆ High Density Interconnect (HDI) Process Could Accommodate High Trace and Component Density
 - Increases PCB cost
 - Used to Reduce Number of PCB Layers and Overall Panel Mass
- ◆ Control and Passive Components Mounted Directly to the Surface of the PCB
- ◆ Approach Offers Potential for Lowest Cost and Mass
- ◆ Technical Challenges Still to be Overcome

SUMMARY

- ◆ Affordability
 - Higher level of manufacturing integration
 - New low power density panel paradigm
- ◆ Efficiency
 - Single chip T/R, minimum combining and interconnect loss
 - Efficient cooling techniques
- ◆ Scalability
 - Highly digital architecture
 - Build arrays to arbitrary size with minimal changes
- ◆ Ground-based application for MDA is a first step towards space, airship, and airborne platforms